CLAIMS

What is claimed is:

1. A process of fabricating a multi-bit charge trapping dielectric flash memory device, comprising:

providing a semiconductor substrate;

forming on the semiconductor substrate a bottom oxide layer and a substrate/oxide interface, wherein the bottom oxide layer comprises a first oxygen concentration and a first nitrogen concentration; and

adding a quantity of nitrogen to the bottom oxide layer, whereby the bottom oxide layer comprises a first region adjacent the charge storage layer and a second region adjacent the substrate/oxide interface, the second region having a second oxygen concentration and a second nitrogen concentration, wherein the second nitrogen concentration exceeds the first nitrogen concentration, provided that the second nitrogen concentration does not exceed the second oxygen concentration.

2. The process of claim 1, wherein the step of adding comprises at least one of (a) annealing the bottom oxide layer in an atmosphere comprising NO, N_2O or NH_3 (b) implanting nitrogen through the bottom oxide followed by annealing, or (c) depositing a nitrogen-containing charge storage layer on the bottom oxide layer to form an ON layer followed by annealing the ON layer.

3. The process of claim 2, wherein the annealing is carried out at a temperature in the range from about 800°C. to about 1150°C.

4. The process of claim 1, wherein the second nitrogen concentration is in the range from about one atomic percent to about 20 atomic percent.

5. The process of claim 1, wherein the first nitrogen concentration is in a range from zero to about 20 atomic percent.

6. The process of claim 1, wherein as a result of the step of adding, the first nitrogen concentration does not substantially change.

7. The process of claim 1, wherein prior to the step of adding, the second region comprises a first number of unsatisfied silicon dangling bonds and silicon-hydrogen bonds and as a result of the step of adding, the first number is reduced to a second number, the second number being smaller than the first number.

8. A process of fabricating a multi-bit charge trapping dielectric flash memory device, comprising:

providing a semiconductor substrate;

forming on the semiconductor substrate a bottom oxide layer and a substrate/oxide interface, wherein the bottom oxide layer comprises a material having a general formula $Si_xO_yN_{z1}$, wherein x, y and z1 are atomic percentages; and

adding a quantity of nitrogen to the bottom oxide layer, whereby the bottom oxide layer comprises a first region adjacent the charge storage layer and a second region adjacent the substrate/oxide interface, whereby the second region comprises a material having a general formula $Si_xO_yN_{z2}$, wherein x, y and z2 are atomic percentages, and $y>z2>z1$.

9. The process of claim 8, wherein the step of adding a quantity of nitrogen comprises at least one of (a) annealing the bottom oxide layer in an atmosphere comprising NO, N_2O or NH_3 (b) implanting nitrogen through the bottom oxide followed by annealing, or (c) depositing a nitrogen-containing charge storage layer on the bottom oxide layer to form an ON layer and annealing the ON layer.

10. The process of claim 9, wherein the annealing is carried out at a temperature in the range from about 800°C. to about 1150°C.

11. The process of claim 8, wherein z2 is in the range from about one atomic percent to about 20 atomic percent.

12. The process of claim 8, wherein following the step of adding, in the first region the values of x, y and z1 remain substantially unchanged.

13. The process of claim 8, wherein z1 is in a range from zero to about 20 atomic percent.

14. The process of claim 8, wherein prior to the step of adding, the second region comprises a first number of unsatisfied silicon dangling bonds and silicon-hydrogen bonds and as a result of the step of adding, the first number is reduced to a second number, the second number being smaller than the first number.

15. A charge trapping dielectric flash memory device, comprising:

a semiconductor substrate having an upper surface;

a bottom oxide layer having a lower surface, the bottom oxide layer formed on the upper surface of the substrate, whereby a substrate/oxide interface is defined by the upper surface and the lower surface; and

a charge trapping dielectric charge storage layer over the bottom oxide layer,

wherein the bottom oxide layer comprises a first region adjacent the charge storage layer and a second region adjacent the substrate/oxide interface, the first region comprising a material having a general formula $Si_xO_yN_{z1}$, the second region comprising a material having a general formula $Si_xO_yN_{z2}$, wherein x, y, z1 and z2 are atomic percentages, and $y > z2 > z1$.

16. The device of claim 15, wherein z2 is in the range from about one atomic percent to about 20 atomic percent.

17. The device of claim 15, wherein z1 is in a range from zero to about 20 atomic percent.

18. The device of claim 15, wherein the charge trapping dielectric material layer comprises a nitride or a high-K dielectric material or a mixture of composite thereof.

19. The device of claim 15 wherein the bottom oxide layer comprises silicon dioxide or a high-K dielectric material or a mixture or composite thereof.

20. The device of claim 15, wherein the bottom oxide layer has a total thickness, and the second region has a thickness equivalent to about 10% to about 50% of the total thickness.